

REMARKS/ARGUMENTS

In answer to his Office Action Examiner's point 4: the Examiner pointed out the existence and relevance of a patent (US 6,766,504) by Rahut et al. This patent teaches a method for optimizing the timing performance of an overall logic circuit implemented in an FPGA. The examiner correctly comments concerning element e) of Claim 1 that "at least the reference teaches routing only one more critical connections of a selected logic level until reaching destination by disregarding other connections or other loads".

This reference refers to the routing of a critical connection with disregard as to other connections or other load. Element e) in the claim refers to "implementing in another way the critical logic performed with relative disregard as to the fanout of signals...and with placement of the logic in the chosen critical path...." The invention intended to be described by the claim is with specific regard to a reimplementation of specifically the logic and not a rerouting of the interconnect with different parameters for a better solution. The idea as described in the disclosure is to place the logic which implements the critical path along the natural path from input signal to output signal. This is described on page 6 lines 9 to 15 of the application in the following manner:

“The more specific method for making these final improvements in logic implementation and logic placement is to take a critical path and implement it using logic gates placed in along the shortest physical path with logic duplicated or moved as needed to achieve optimal implementation of that path. Any logic which is involved with other critical paths is replicated with the original logic left in place; any logic which is involved in only this specific critical path is simply moved.”

Thus, these words describe the implementation of the logic, and not the routing which utilizes routing resources. In the Xilinx handbooks these are referred to as “logic elements” which are a separate resource with respect to the routing resources.

With regards to point 4 by the examiner regarding claim 1, the claim is amended in step e) to clarify that logic elements chosen to implement the critical path are being changed.

With regards to point 5 by the examiner regarding claims 2 and 4, the word “logic” is replaced by the words “logic elements” to clarify that the placement of logic elements is included, and not simply a reroute utilizing different routing resources.

With regards to point 6 by the examiner regarding claim 3, the claim is amended in step e) in the same manner described for point 4 regarding claim 1 to clarify that logic elements chosen to implement the critical path are being changed.

The undersigned agent appreciates the close scrutiny by the Examiner of the original application and also appreciates the necessity of clarifying the scope of the claims.

In view of these Remarks/Arguments and the amendments to the Claims, it is respectfully believed that the case is now in condition for allowance, and an early notice to that effect is earnestly solicited.

Respectfully submitted,



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